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Claims searched: 1 to 22

Examiner: Peter Easterfield
Date of search: 28 February 2001

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

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Int Cl (Ed.7): H03H 1/00, 3/00, 7/30, 7/32, 7/34

Other: Online; WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0675560 A1	(MURATA)	
X	US 5436601 A	(MANDAI et al) see figs 6 & 7	1-5,10-12, 14-19,22
A	US 4203081 A	(BRAECKELMANN)	

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

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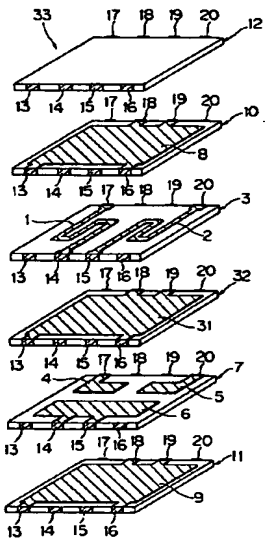
(54) Low-pass filter.

(57) A low-pass filter is obtained by inserting a third dielectric substrate (32) having a shielding electrode (31) on its upper surface between a first dielectric substrate (3) having microstriplines (1, 2) on its upper surface and a second dielectric substrate (7) having capacitor electrodes (4 to 6) on its upper surface, stacking fourth and fifth dielectric substrates (11, 10) having ground electrodes (8, 9) on upper surfaces thereof on both sides of the first to third dielectric substrates, and stacking a dielectric sheet (12) on the uppermost portion.

FIG. 1



EP 0 675 560 A1

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a low-pass filter which is suitably applied to a high-frequency circuit, and more particularly, it relates to a low-pass filter employing a multilayered chip which is formed by stacking a plurality of dielectric layers with each other.

Description of the Background Art

A well-known low-pass filter is described with reference to Figs. 5 and 6. Fig. 5 is an exploded perspective view showing a conventional low-pass filter 130, and Fig. 6 is a perspective view showing the appearance of this low-pass filter 130.

The low-pass filter 130 is formed by a multilayered chip, which is obtained by stacking dielectric substrates 103, 107, 110 and 111 and a dielectric sheet 112 with each other.

The dielectric substrate 103 is provided on its upper surface with microstriplines 101 and 102, which are in the form of folded straight lines. On the other hand, the dielectric substrate 107 is provided on its upper surface with capacitor electrodes 104 to 106. These dielectric substrates 103 and 107 are held between the dielectric substrates 110 and 111.

The dielectric substrates 110 and 111 are provided on upper surfaces thereof with ground electrodes 108 and 109 respectively.

This multilayered chip can be obtained by properly forming the aforementioned electrode structures on dielectric green sheets, thereafter stacking the green sheets with each other, and integrally firing the ceramic material with the electrode material. Alternatively, fired dielectric substrates may be employed to define the dielectric substrates 103, 107, 110 and 111 respectively.

External electrodes 113 to 116 are formed on first longer side surfaces of the dielectric substrates 103, 107, 110 and 111 and the dielectric sheet 112, while external electrodes 117 to 120 are formed on second side surfaces thereof respectively. As clearly understood from Fig. 6, these external electrodes 113 to 120 are formed on longer side surfaces of a multilayered chip 131 as finally obtained, and Fig. 5 shows the same in parted states.

As clearly understood from Figs. 5 and 6, ends of the microstripline 101 are electrically connected with the external electrodes 114 and 117 respectively. On the other hand, ends of the external electrode 102 are electrically connected with the external electrodes 115 and 120 respectively. The capacitor electrode 104 is electrically connected with the external electrode 117, while the capacitor electrode 105 is electrically connected with the external electrode 120. Further, the capacitor electrode 106 is electrically connected with the external electrodes 114 and 115. In addition, the ground electrode 108 is electrically connected with the external electrodes 113, 116, 118 and 119, while the ground electrode 109 is also electrically connected with the external electrodes 113, 116, 118 and 119.

The microstriplines 101 and 102 are adapted to form inductance components, i.e., inductances L1 and L2 appearing in an equivalent circuit shown in Fig. 7, respectively.

Further, the capacitor electrodes 104 to 106 form capacitors C1 to C3 appearing in the equivalent circuit shown in Fig. 7 with the ground electrode 109 respectively.

The dielectric sheet 112 is adapted to protect the ground electrode 108 which is provided on the dielectric substrate 110.

In this low-pass filter 130, the external electrodes 117 and 120 are employed as input and output ends respectively. Further, the external electrodes 113, 116, 118 and 119 are connected with the ground potential. The external electrode 114 is adapted to electrically connect the end of the microstripline 101 with the capacitor electrode 106. Similarly, the external electrode 115 is adapted to electrically connect an end of the microstripline 102 with the capacitor electrode 106.

When the external electrodes 117 and 120 are employed as input and output ends respectively and the external electrodes 113, 116, 118 and 119 are employed as portions connected to the ground potential, therefore, the low-pass filter 130 can operate as that of the equivalent circuit shown in Fig. 7.

Fig. 8 shows the transmission characteristic of the low-pass filter 130. As clearly understood from Fig. 8, insertion loss is damped in the position of the resonance frequency, and thereafter increased in a frequency band higher than the resonance frequency. Such increase of the insertion loss in the high frequency band is caused since a high-frequency signal bypasses the microstriplines 101 and 102 by floating capacitances which are developed across the microstriplines 101 and 102 respectively. Consequently, it is difficult to remove an unnecessary high-frequency signal.

In order to shift the passband of the low-pass filter 130 toward the low frequency side, the resonance frequency of the low-pass filter 130 may be reduced. In order to reduce the resonance frequency, however, it is necessary to increase the lengths of the microstriplines 101 and 102 for increasing the values of the inductances L1 and L2, or to increase the areas of the capacitor electrodes

104 and 106 for setting electrostatic capacitances of the capacitors C1 to C3. In this case, the low-pass filter 130 is disadvantageously increased in size.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems of the prior art, an object of the present invention is to provide a low-pass filter which can increase the amount of damping of a signal passing through the low-pass filter in a high frequency region by reducing a floating capacitance developed across a microstrip line, and which can be miniaturized as a whole.

According to a wide aspect of the present invention, provided is a low-pass filter employing a multilayered chip obtained by stacking a plurality of dielectric layers with each other. This low-pass filter comprises a first dielectric substrate having a microstripline on its one surface, a second dielectric substrate which is provided with a capacitor electrode on its one surface, a third dielectric substrate which is provided with a shielding electrode on its one surface and arranged between the first and second dielectric substrates, a dielectric sheet which is directly or indirectly stacked on a first surface of a multilayer structure obtained by stacking the first to third dielectric substrates with each other, and a fourth dielectric substrate which is provided with a ground electrode on its one surface and stacked on a second surface of the multilayer structure which is opposite to the first surface, while the ground electrode is electrically connected with the shielding electrode.

In this case, a first capacitor is formed by the capacitor electrode and the ground electrode while a second capacitor is formed by the capacitor electrode and the shielding electrode, so that the second capacitor is connected in parallel with the first capacitor. Similarly to the conventional low-pass filter, the microstripline forms an inductance.

In the low-pass filter according to the present invention, the third dielectric substrate having the shielding electrode is inserted between the first dielectric substrate having the microstripline for forming an inductance and the second dielectric substrate having the capacitor electrode, whereby it is possible to reduce a floating capacitance which is developed across the microstripline. Therefore, the amount of damping in a high frequency region can be increased in a signal passing through the low-pass filter, thereby effectively removing an unnecessary high-frequency signal.

According to the present invention, further, the second capacitor is formed by the capacitor electrode and the shielding electrode so that the second capacitor is added in parallel to the first capacitor, thereby doubling the total electrostatic capacitance of the capacitors. Thus, it is possible to reduce the resonance frequency of the low-pass filter without increasing its size. When the low-pass filter is obtained with a constant resonance frequency, it is possible to provide a low-pass filter which is smaller in size than the conventional one.

According to a specific aspect of the present invention, a fifth dielectric substrate which is provided with a ground electrode on its one surface is inserted between the dielectric sheet and the first surface of the multilayer structure. Due to such insertion of the fifth dielectric substrate, it is possible to effectively shield a principal part of the low-pass filter against external noises by the ground electrode which is formed on the fifth dielectric substrate.

According to another specific aspect of the present invention, at least three external electrodes are formed on outer surfaces of the multilayered chip, so that these at least three external electrodes are electrically connected with any ones of the microstripline, the capacitor electrode and the ground electrode provided in the exterior, to form a π filter.

According to the present invention, the electrical connection between the ground electrode and the shielding electrode may be attained through an external electrode which is formed on an outer surface of the multilayered chip. Alternatively, a viahole electrode may be formed in the multilayered chip so that the ground electrode is electrically connected with the shielding electrode through this viahole electrode.

Further, an end of the microstripline may be connected with the ground electrode through the viahole electrode which is formed in the multilayered chip.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is an exploded perspective view showing a low-pass filter according to a first embodiment of the present invention;

Fig. 2 is a perspective view showing the appearance of the low-pass filter according to the first embodiment of the present invention;

Fig. 3 illustrates the transmission characteristic of the low-pass filter shown in Fig. 1;

Fig. 4 is an exploded perspective view showing a low-pass filter according to a second embodiment of the present invention;

Fig. 5 is an exploded perspective view showing a conventional low-pass filter;

Fig. 6 is a perspective view showing the appearance of the low-pass filter shown in Fig. 4;

Fig. 7 is an equivalent circuit diagram of the low-pass filter shown in Fig. 4; and

Fig. 8 illustrates the transmission characteristic of the low-pass filter shown in Fig. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Some embodiments of the inventive low-pass filter are now described with reference to the drawings. The feature of the present invention resides in that a third dielectric substrate which is provided with a shielding electrode on its one surface is inserted between a first dielectric substrate which is provided with a microstripline and a second dielectric substrate which is provided with a capacitor electrode on its one surface.

Fig. 1 is an exploded perspective view showing a low-pass filter 33 according to a first embodiment of the present invention, and Fig. 2 is a perspective view showing its appearance.

As shown in Fig. 1, a first dielectric substrate 3, a second dielectric substrate 7, a third dielectric substrate 32, a fourth dielectric substrate 11, a fifth dielectric substrate 10, and a dielectric sheet 12 are stacked with each other to form a multilayered chip 34, in the low-pass filter 33 according to this embodiment.

The first dielectric substrate 3 is provided on its upper surface with microstriplines 1 and 2 which are in the form of folded straight lines. On the other hand, capacitor electrodes 4 to 6 are formed on an upper surface of the second dielectric substrate 7. Further, a shielding electrode 31 is formed on an upper surface of the third dielectric substrate 32. In addition, ground electrodes 9 and 8 are formed on upper surfaces of the fourth and fifth dielectric substrates 11 and 10 respectively.

As clearly understood from Fig. 2, external electrodes 13 to 16 are formed on one longer side surface of the multilayered chip 34, while external electrodes 17 to 20 are formed on another side surface thereof. Referring to Fig. 1, these external electrodes 13 to 20 are illustrated in states parted on side surfaces of the dielectric substrates 3, 7, 10, 11 and 32 and the dielectric sheet 12 respectively.

The dielectric substrates 3, 7, 10, 11 and 32 can be formed by previously fired dielectric ceramic substrates or plates of another proper dielectric material. Alternatively, the multilayered chip 34 may be obtained by applying conductive paste onto upper surfaces of dielectric ceramic green sheets for forming the respective electrodes, stacking the green sheets with each other and integrally firing the same.

Ends of the microstripline 1 are electrically connected with the external electrodes 17 and 14 respectively, while ends of the microstripline 2 are electrically connected with the external electrodes 15 and 20 respectively. The microstriplines 1 and 2 are adapted to form inductances L1 and L2 in a low-pass filter of an equivalent circuit shown in Fig. 7 respectively.

The capacitor electrodes 4 to 6 overlap with the ground electrode 9 through the dielectric substrate 7. Therefore, first capacitors are formed by the capacitor electrodes 4 to 6 and the ground electrode 9 respectively. According to this embodiment, further, the capacitor electrodes 4 to 6 are opposed to the shielding electrode 31 through the dielectric substrate 32. Thus, second capacitors are formed by the capacitor electrodes 4 to 6 and the shielding electrode 31 respectively.

The shielding electrode 31 is electrically connected with the external electrodes 13, 16, 18 and 19. Similarly, the ground electrodes 9 and 8 are also electrically connected with the external electrodes 13, 16, 18 and 19.

In the low-pass filter 33 according to this embodiment, the external electrodes 17 and 20 are employed as input and output ends respectively, while the external electrodes 13, 16, 18 and 19 are connected with the ground potential. Therefore, it is possible to implement a low-pass filter circuit which is similar to that formed by the LC circuit shown in Fig. 7. According to this embodiment, further, the second capacitors are formed by the capacitor electrodes 4 to 6 and the shielding electrode 31, in addition to the first capacitors which are formed by the capacitors 4 to 6 and the ground electrode 9 respectively. Therefore, the respective capacitors are added in parallel to the respective first capacitors, whereby electrostatic capacitances of the capacitors C1 to C3 are doubled as compared with the prior art shown in Fig. 4. Thus, it is possible to reduce the resonance frequency of the low-pass filter 33.

Fig. 3 shows the filter characteristic of the low-pass filter 33 according to this embodiment in a solid line, and that of the conventional filter shown in Fig. 5 in a broken line. It is clearly understood from Fig. 3 that the conventional low-pass filter attains an amount of damping of -20 dB, for example, merely in the frequency band up to the frequency of 6.5 GHz. On the other hand, the low-pass filter 33 according to this embodiment can attain an amount of damping of -20 dB up to the frequency of 10.5 GHz.

Further, the resonance frequencies of the conventional low-pass filter and the low-pass filter 33 according to this embodiment are 2.2 GHz and 1.8

GHz respectively. Thus, it is understood possible to reduce the resonance frequency by 18 % according to the present invention.

The fifth dielectric substrate 10 shown in Fig. 1 is simply adapted to shield the low-pass filter 33 against external noises, and not requisite for the present invention. Namely, this dielectric substrate 10 may be omitted.

A low-pass filter 70 according to a second embodiment of the present invention is now described with reference to Fig. 4.

Fig. 4 is an exploded perspective view showing the low-pass filter 70 according to the second embodiment of the present invention, in correspondence to Fig. 1 showing the first embodiment.

In the low-pass filter 70 according to the second embodiment, a first dielectric substrate 43, a second dielectric substrate 47, a third dielectric substrate 49, a fourth dielectric substrate 53, a fifth dielectric substrate 52, and a dielectric sheet 54 are stacked with each other to form a multilayered chip.

The second embodiment is different from the first embodiment in a point that first ends of microstriplines 41 and 42 which are formed on the first dielectric substrate 43 are electrically connected with viahole electrodes 64, while not reaching an edge of the dielectric substrate 43. The viahole electrodes 64 pass through the dielectric substrates 43 and 49, to be electrically connected with a capacitor electrode 46. In the dielectric substrate 49, holes 65 are formed in a shielding electrode 48 in order to prevent short-circuiting across the shielding electrode 48 and the viahole electrodes 64.

According to this embodiment, further, viahole electrodes 66 are formed in the multilayered chip. These viahole electrodes 66 are so formed as to pass through the dielectric substrates 52, 43, 49 and 47, for electrically connecting a ground electrode 50, the shielding electrode 48 and another ground electrode 51 with each other.

Thus, the shielding electrode 48 is so formed on the third dielectric substrate 49 that its outer peripheral edges do not reach edges of the dielectric substrate 49. The ground electrode 50 is also formed on the fifth dielectric substrate 52 not to reach outer peripheral edges of the dielectric substrate 52.

Also in this embodiment, external electrodes 55 to 58 and 59 to 62 are formed on longer side surfaces of the multilayered chip respectively. Among the external electrodes 55 to 62, the external electrodes 55, 58, 60 and 61 are electrically connected with the ground electrode 51. Therefore, the ground electrode 50 and the shielding electrode 48 are electrically connected with the external electrodes 55, 58, 60 and 61, due to the electrical connection with the ground electrode 51 through the viahole electrodes 66.

On the other hand, second ends of the microstriplines 41 and 42 reaching another edge of the dielectric substrate 43 are connected with the external electrodes 59 and 62 respectively. The first ends of the microstriplines 41 and 42 are electrically connected with the capacitor electrode 46 by the aforementioned viahole electrodes 64. Further, capacitor electrodes 44 and 45 are electrically connected with the external electrodes 59 and 62 respectively. In addition, the second ends of the microstriplines 41 and 42 are electrically connected with the capacitor electrodes 44 and 45 respectively by viahole electrodes 63 which are formed in the vicinity of the outer edge of the dielectric substrate 43.

Also in this embodiment, therefore, it is possible to form the low-pass filter 70 similarly to the first embodiment by employing the external electrodes 59 and 62 as input and output ends respectively and connecting the external electrodes 55, 58, 60 and 61 with the ground potential, for attaining an effect which is similar to that of the first embodiment.

Namely, the feature of the low-pass filter 70 according to the second embodiment of the present invention resides in that the electrical connection between the microstriplines 41 and 42, the ground electrodes 50 and 51, the shielding electrode 48 and the capacitor electrodes 44 to 46 is attained by the viahole electrodes 63, 64 and 66. In other words, the electrical connection is at least partially attained by the viahole electrodes which are formed in the multilayered chip according to this embodiment, while that between the respective electrodes is entirely attained by the external electrodes which are formed on the outer surfaces of the multilayered chip in the low-pass filter 30 according to the first embodiment. The remaining points of this embodiment are similar to those of the first embodiment.

Also in the second embodiment, the fifth dielectric substrate 52 may be omitted. However, it is possible to preferably shield the low-pass filter 70 against external noises by inserting the fifth dielectric substrate 52.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Claims

1. A low-pass filter employing a multilayered chip being obtained by stacking a plurality of dielectric layers with each other, said low-pass filter comprising:

   a first dielectric substrate having a microstripline on its one surface;

   a second dielectric substrate being provided with a capacitor electrode on its one surface;

   a third dielectric substrate being provided with a shielding electrode on its one surface and arranged between said first and second dielectric substrates;

   a dielectric sheet being directly or indirectly stacked on a first surface of a multilayer structure being obtained by stacking said first to third dielectric substrates with each other; and

   a fourth dielectric substrate being provided with a ground electrode on its one surface and stacked on a second surface of said multilayer structure being opposite to said first surface,

   said ground electrode being electrically connected with said shielding electrode.

2. The low-pass filter in accordance with claim 1, wherein a first capacitor is formed by said capacitor electrode and said ground electrode, and a second capacitor is formed by said capacitor electrode and said shielding electrode, said second capacitor being connected in parallel with said first capacitor.

3. The low-pass filter in accordance with claim 1 or 2, further comprising a fifth dielectric substrate being provided with a second ground electrode on its one surface and arranged between said dielectric sheet and said first surface of said multilayer structure.

4. The low-pass filter in accordance with claim 1, further comprising an external electrode being formed on an outer surface of said multilayered chip, said external electrode being electrically connected with any one of said microstripline, said capacitor electrode, said ground electrode and said shielding electrode.

5. The low-pass filter in accordance with claim 4, wherein at least three external electrodes are formed on said outer surface of said multilayered chip, for forming a π filter.

6. The low-pass filter in accordance with claim 4, wherein said electric connection between said ground electrode and said shielding electrode is formed by said external electrode being formed on said outer surface of said multilayered chip.

7. The low-pass filter in accordance with claim 4, wherein a viahole electrode is formed in said multilayered chip, said ground electrode being electrically connected with said shielding electrode by said viahole electrode.

8. The low-pass filter in accordance with claim 4, wherein a viahole electrode is formed in said multilayered chip, an end of said microstripline being electrically connected with said capacitor electrode by said viahole electrode.

FIG. 1

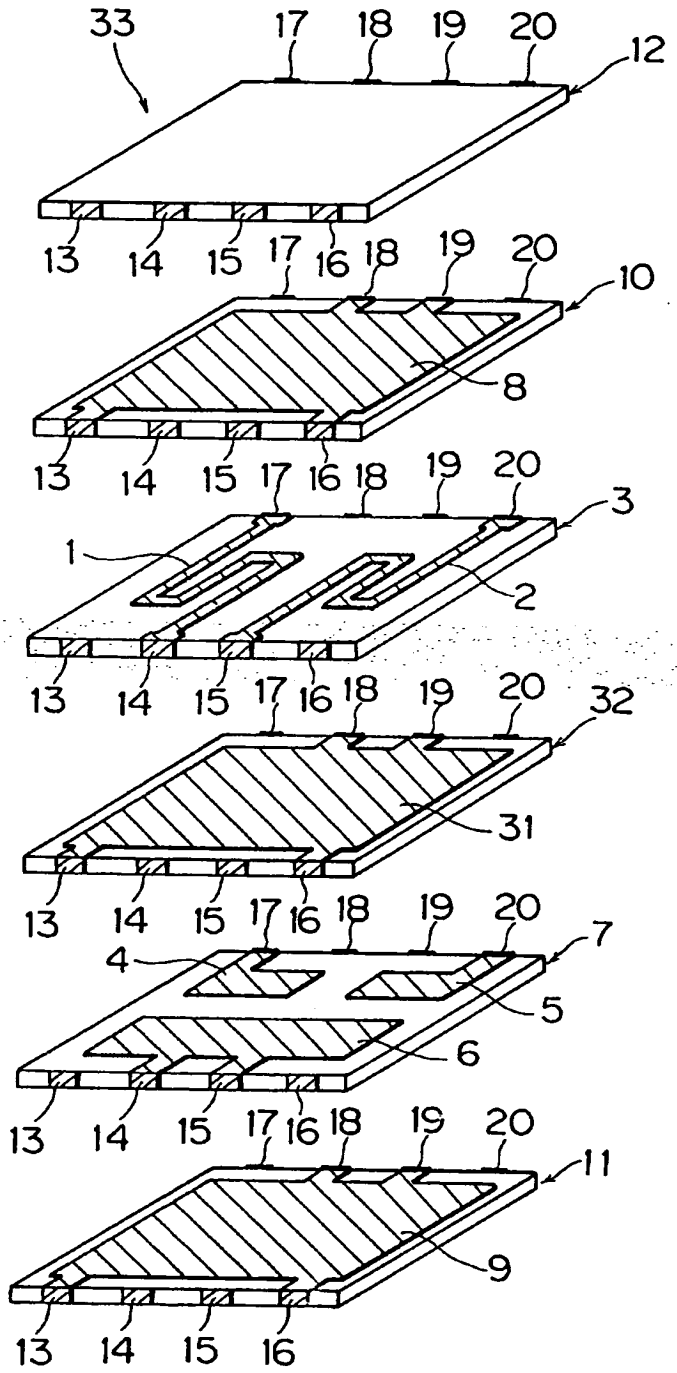


FIG. 2

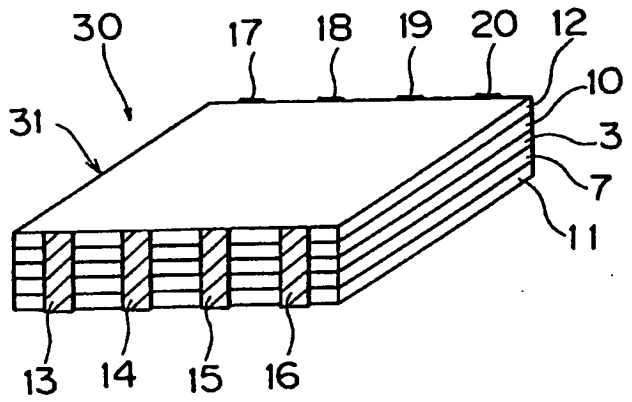

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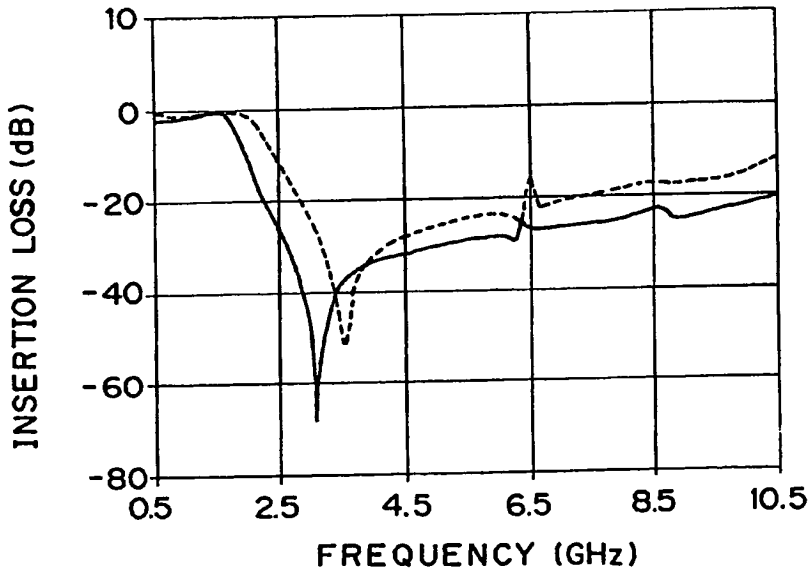
FIG. 3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FREQUENCY (GHz)

FIG.4

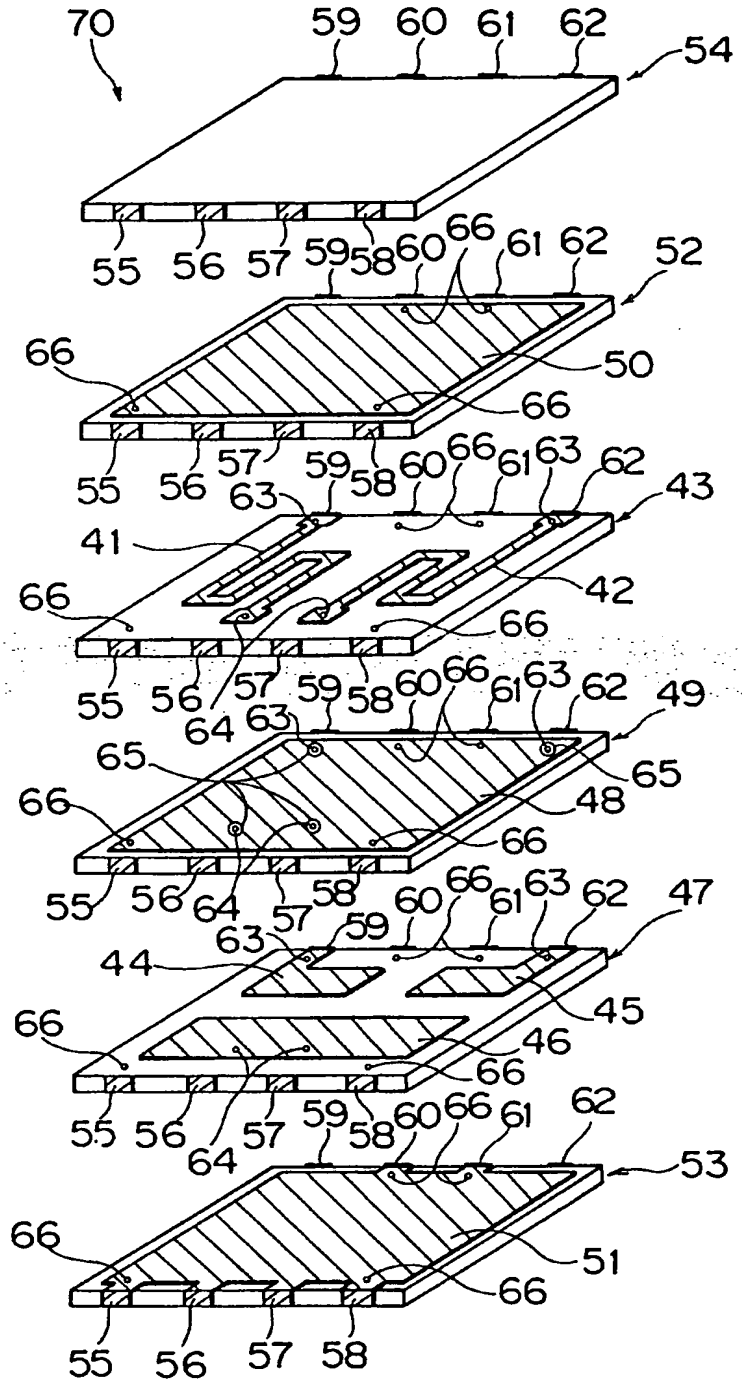
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FIG. 5

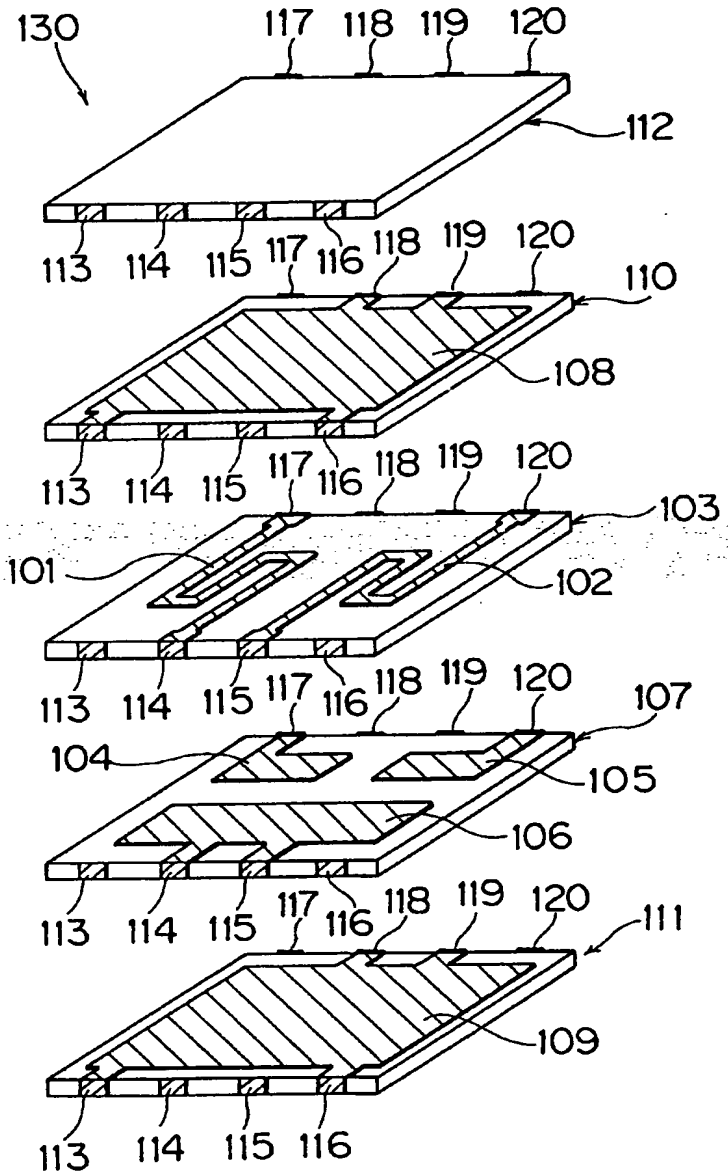
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FIG. 6

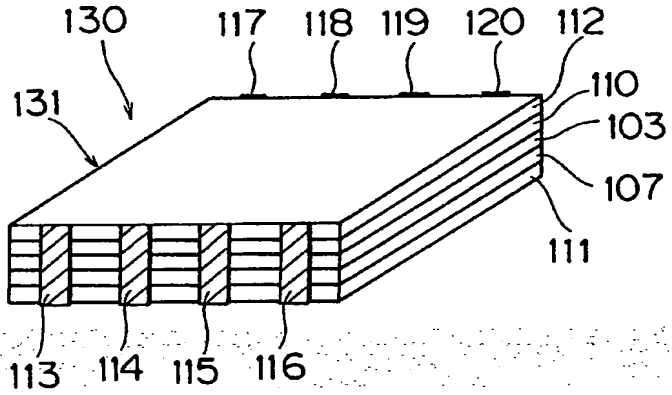
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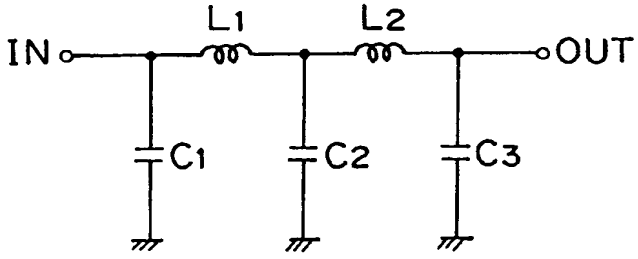
FIG. 7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OUT
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C2
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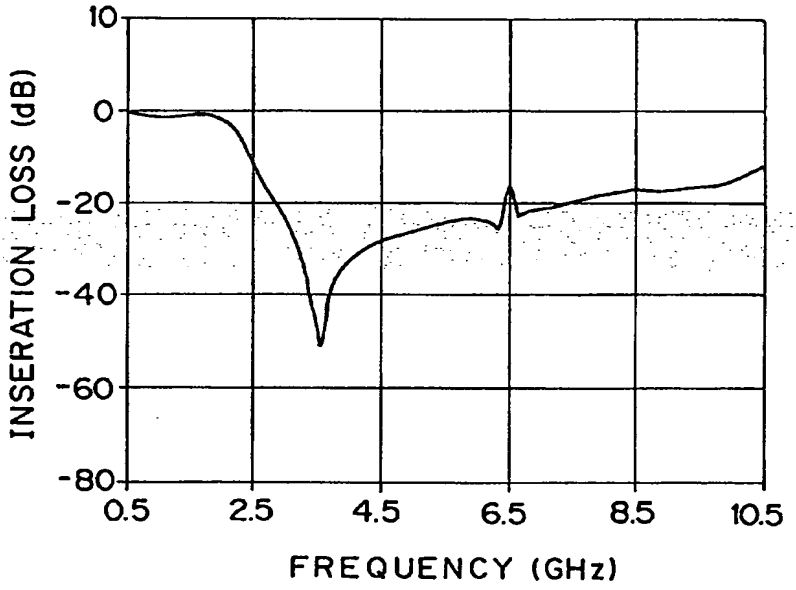
FIG. 8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4.5
6.5
8.5
10.5
FREQUENCY (GHz)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 10 4332

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 566 145 (MURATA MANUFACTURING CO. LTD.) * column 5, line 17 - column 7, line 37; figure 2 *	1,3-6	H01P1/203
A	DE-A-41 19 551 (MURATA MANUFACTURING CO. LTD.) * column 5, line 18 - column 6, line 36; figure 3 *	1,2,8	
A	US-A-2 812 501 (SOMMERS) * column 2, line 11 - line 34; figure 1 *	7	
P,L, X	DE-A-44 01 173 (MURATA MANUFACTURING CO. LTD.) * column 2, line 33 - column 3, line 45; figures 1,2 *	1-8	
P,X	EP-A-0 641 035 (MATSUSHITA ELECTRIC IND. CO. LTD.) * page 31, line 52 - page 32, line 26; figure 42 *	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)
H01P
H03H

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 June 1995	Den Otter, A

CATEGORY OF CITED DOCUMENTS
X : particularly relevant if taken alone
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P : intermediate document

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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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